LPC2478: 内置液晶控制接口的单芯片系统解决方案

微控制器产品
多重市场半导体
恩智浦半导体

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- LPC2478简介
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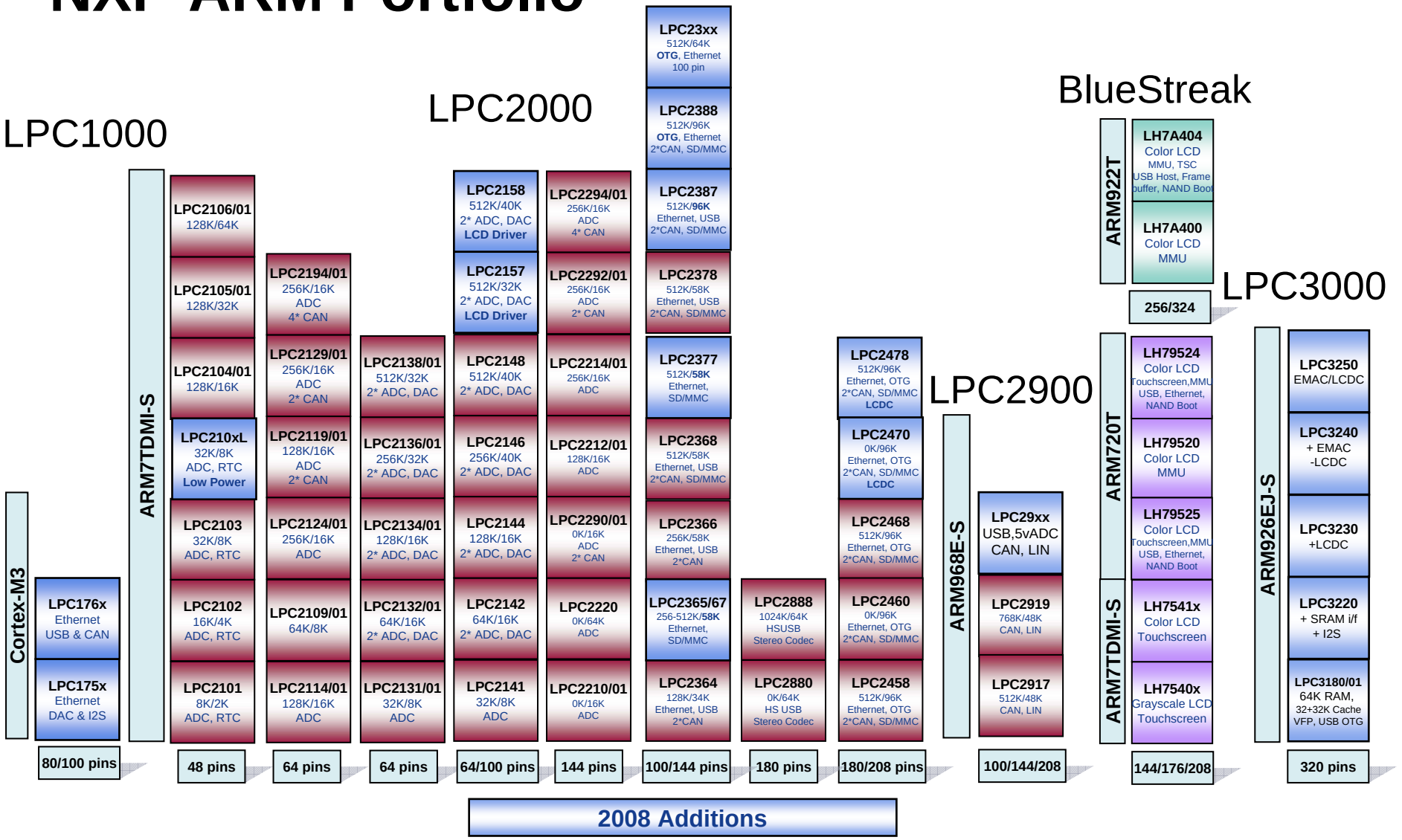
LPC2000 简介

NXP ARM Portfolio



80 ARM MCUs by the end of 2008!

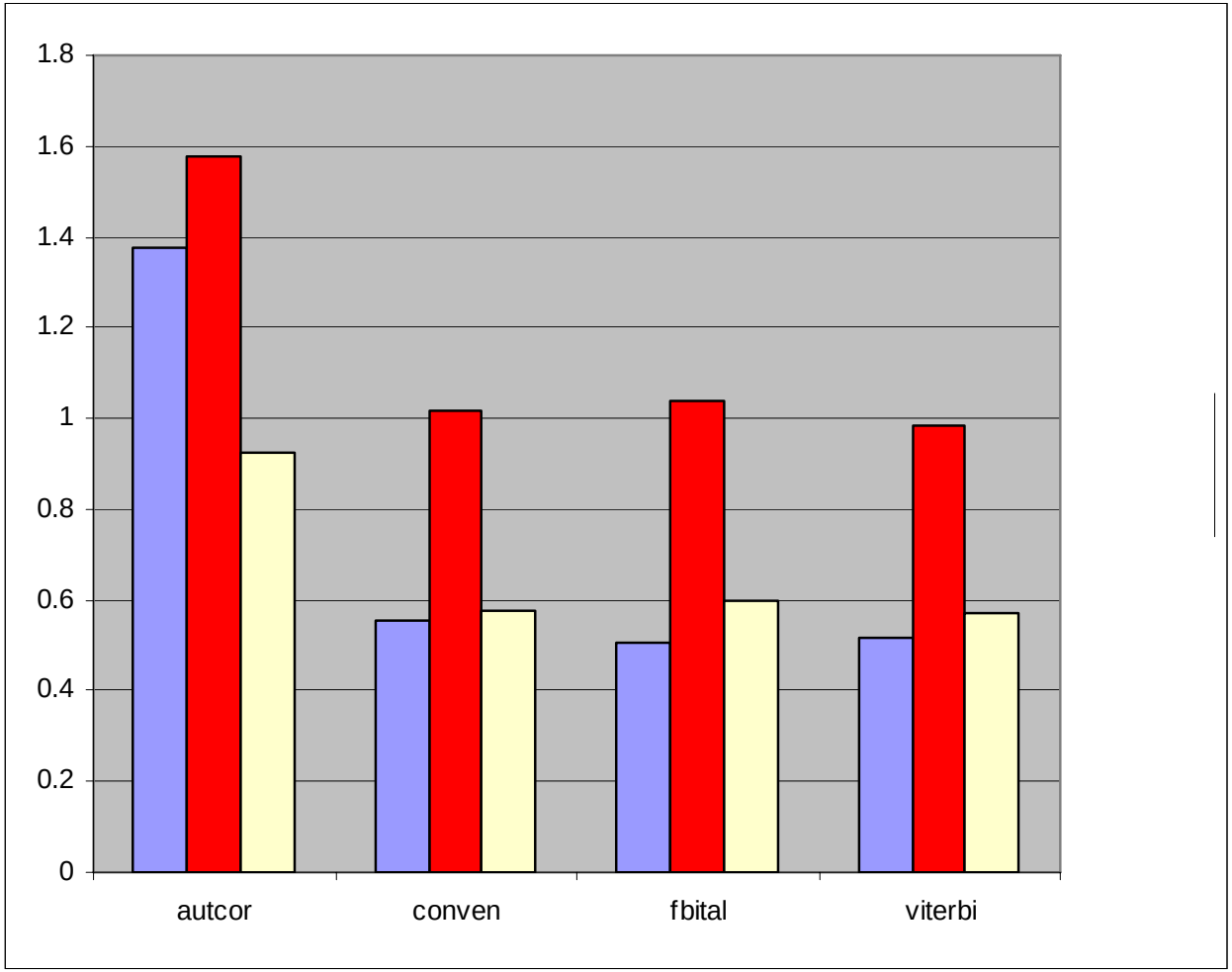
Best Flash in the Market

"In all seven benchmark tests, the NXP LPC2129 showed a consistent performance edge of 37 percent to 51 percent compared with the other ARM7-based devices, demonstrating the impact of the LPC2129's optimized flash interface."

-November 8, 2006: EEMBC® Scores for NXP's ARM7-Based LPC2129 Show Dramatic Effect of Memory Subsystem on Microcontroller Performance

http://www.eembc.org/

EEMBC ARM7 Performance Benchmark



- **NXP LPC2129**
- **Competitor A**
- **Competitor B**

- Microcontrollers all running the SAME IAR compiled EEMBC Telecom code

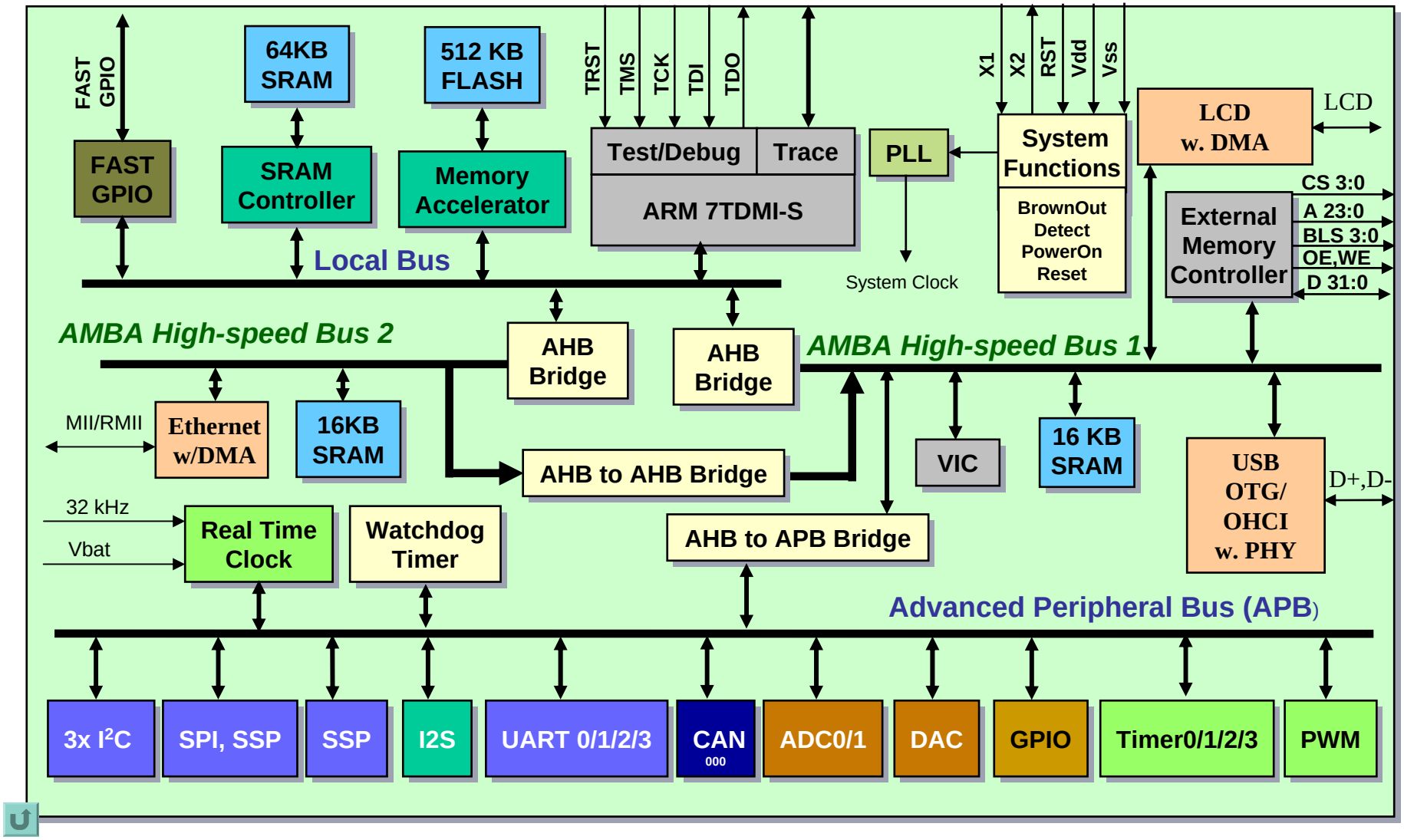
LPC2478 简介

LPC246x and LPC247x series

- All of the features of the LPC2368 **PLUS**:
- USB OTG/ Host (OHCI)
- External Memory Interface
  - Interface up to 4 banks of 16 MB external memory
- 98 KB Total SRAM
- Ethernet MAC has MII interface in addition to RMII
- XGA LCD Controller (LPC2470 and LPC2478 only)
- LQFP and TFBGA 208 packages (TFBGA180 for LPC2458)
- Evaluation Boards from Embedded Artists

	Flash	Total RAM	Ext Memory Interface	LCD Controller	Package	Release Date
LPC2458	512 KB	98 KB	16-bit	No	TFBGA180	Q1 08
LPC2460	0 KB	98 KB	32-bit	No	LQFP208, TFBGA208	Q1 08
LPC2468	512 KB	98 KB	32-bit	No	LQFP208, TFBGA208	Now
LPC2470	0 KB	98 KB	32-bit	Yes	LQFP208, TFBGA208	Q1 08
LPC2478	512 KB	98 KB	32-bit	Yes	LQFP208, TFBGA208	Q1 08

LPC247x Block Diagram



The Challenge

- An MCU may be required to collect data, issue control signals and move data across a network in real time via Ethernet, CAN and/or USB. A single bus MCU architecture is bogged down with these tasks.
- Now that end users demand higher performance graphics and more highly integrated displays – high quality graphics are a must. The continuous feeding of the LCD with ever-changing data will completely overwhelm a single bus ARM7 MCU.
- The dual-AHB bus structure of the LPC2300 and LPC2400 families reduces this burden
  - Allows concurrent operation of the zero wait-state Flash, 10/100 Ethernet and LCD

Independent Buses - the LPC247x Advantage

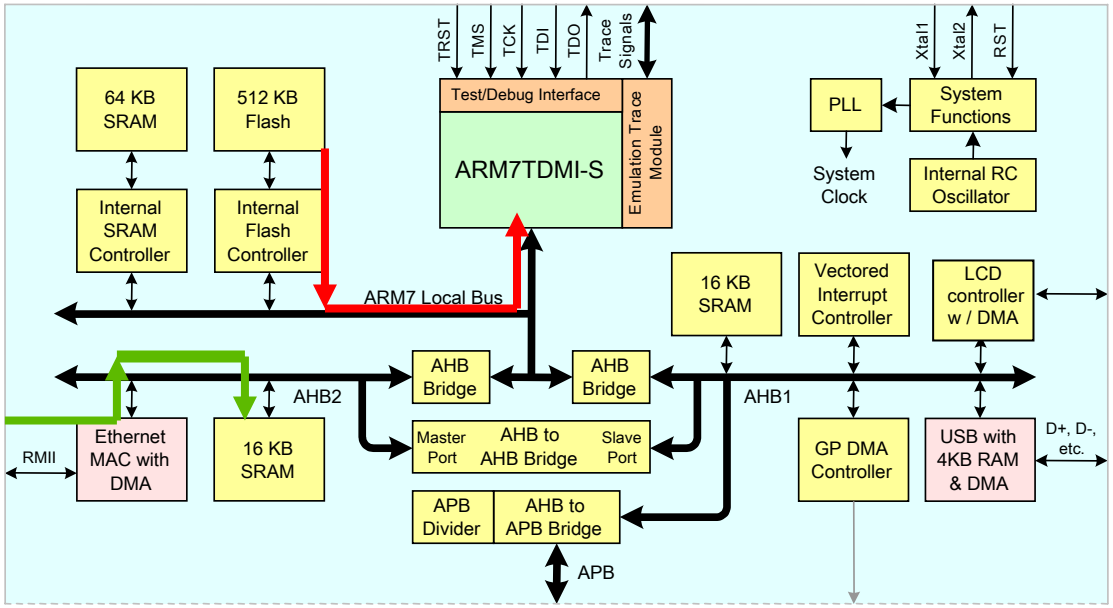
- With independent Local, AHB1 and AHB2 buses, concurrent operations become possible
- Local Bus connects CPU with zero wait-state Flash
  - CPU Instruction Fetch
- AHB1 bus support USB OTG/OHCI/Device and LCD
  - USB packet reception and transfer to SRAM
  - 4 KB FIFO Buffer for USB
  - LCD frame transfer from internal or external SRAM
  - 16 KB SRAM for USB or LCD buffering of heavy traffic
  - USB DMA and LCD DMA
- AHB2 Dedicated to Ethernet
  - Ethernet packet reception and transfer to SRAM
  - 16 KB SRAM for Ethernet buffering
  - Ethernet DMA

The LPC247x Advantage - parallel buses

Concurrent operations become possible:

- Ethernet packet reception and transfer to SRAM
- CPU Instruction Fetch
- LCD frame reception and transfer to SRAM

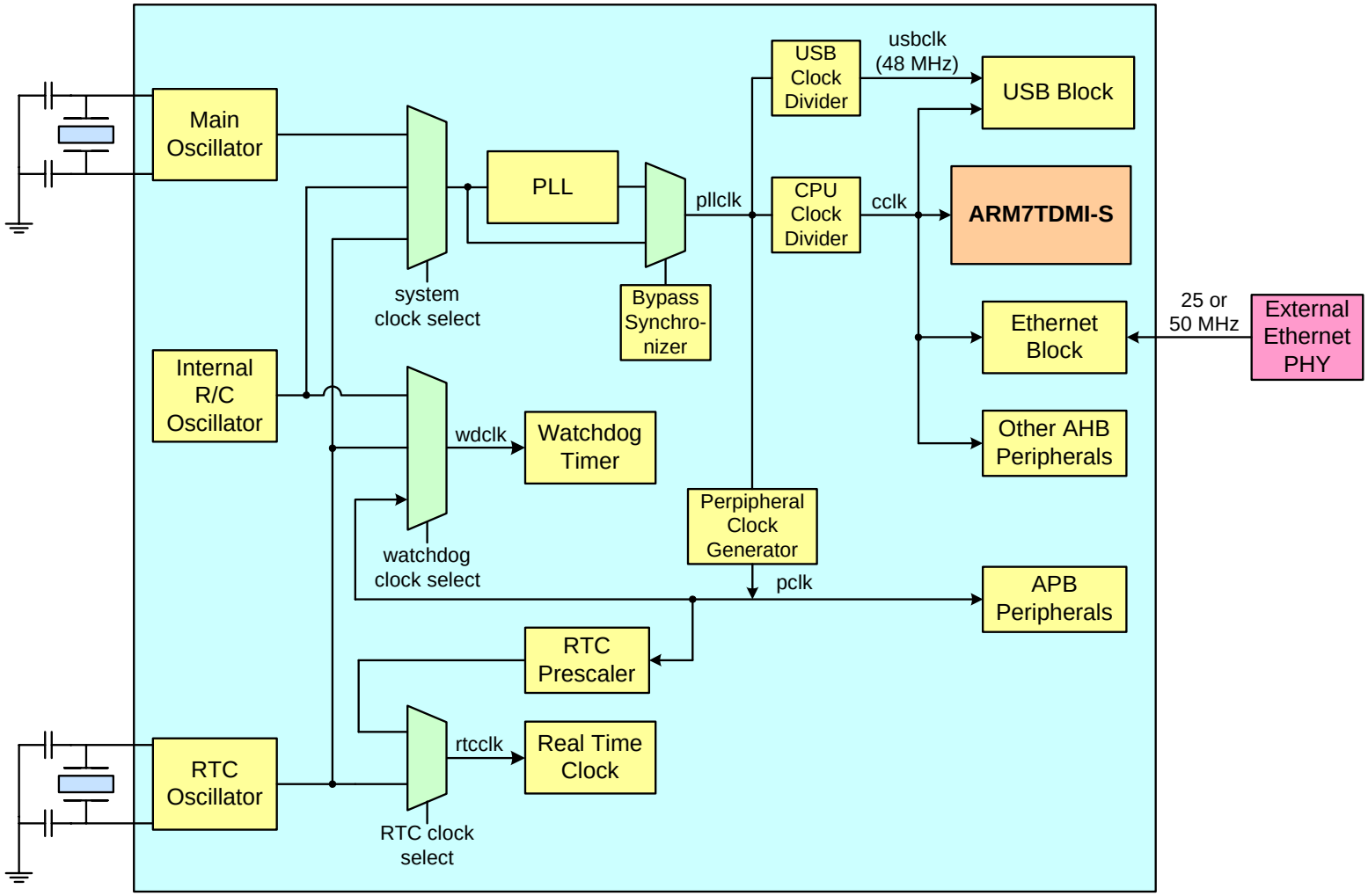
Dedicating AHB Bus to Ethernet is required to guarantee 100 Mbits/sec Ethernet throughput without contention with other peripherals



LPC247x – CPU & Memory

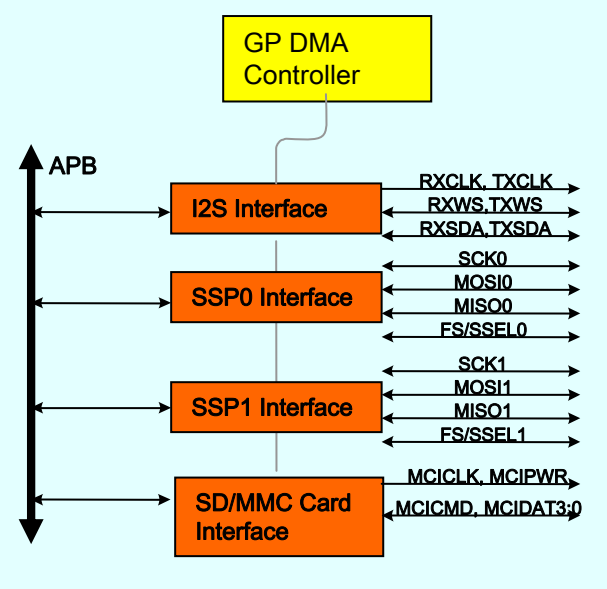
- ARM7TDMI-S Processor – 72 MHz
- 512 KB Flash on-chip Flash (LPC2478 only)
  - zero wait-state (execute code from Flash or SRAM)
  - 128-bit wide bus with patented Memory Accelerator Module (MAM)
  - 8-bits Error Correction Code (ECC) for every 128-bit word
  - Automotive qualified Flash process for high reliability
- 98 KB on-chip Static RAM
  - 64 KB SRAM exclusively for CPU
  - 16 KB for Ethernet buffering
  - 16 KB for USB or LCD
  - 2 KB for RTC is for data only
  - Additional 4 KB USB FIFO buffer
- Advanced Vectored Interrupt Controller (VIC) – 32 IRQ sources
- Emulation Trace Module supports real-time trace
- Low power - 3 reduced power modes

Building the LPC247x – Clock Source



General Purpose DMA

- General Purpose two-channel DMA supports high-speed peripherals as well as memory-to-memory transfers
  - 32-bit AHB master bus width (support 8-, 16-, or 32-bit transfers)
  - Internal four-word FIFO per channel
- Can be used with SD/MMC, two SSP and the I^2S interface
  - Connect peripherals to each other or to memory
- Flexible, customizable DMA performance
  - Big-endian and little-endian support
  - Programmable DMA burst size
  - Hardware DMA channel priority
  - Can generate interrupts



LPC247x External Memory Interface

- MultiPort Memory Controller peripheral that offers support for SRAM, ROM, Flash, and memory-mapped peripherals
  - Four chip selects each for synchronous and static memory devices
  - Supports 2K, 4K, and 8K row address synchronous memory parts
  - Asynchronous page mode read
  - Programmable Wait States
  - Bus turnaround delay
  - Output enable and write enable delays
  - Extended Wait
- Also supports SDRAM with 16-bit and 32-bit wide chip select
  - Power saving modes control CKE and CLKOUT
  - Self-refresh mode controlled by software
- Read and Write buffers improve performance and reduce latency
- 8/16/32 data lines and 24 address lines

LPC247x Peripherals

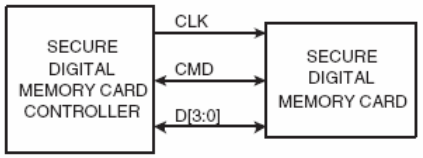
- 10/100 Ethernet
  - Built in MAC with MII and RMII interfaces to external PHY
  - 16 KB SRAM for heavy traffic buffering
  - Ethernet DMA
- USB 2.0 Full Speed On-The-Go/Open Host Control Interface/Device
  - Built in Device and OHCI PHY
  - USB DMA
  - 16 KB SRAM Buffer + 4 KB FIFO
  - Supports 32 endpoints and all transfer modes
- CAN 2.0B
  - Two channels
  - Built-in Hardware Acceptance Filters
- I^2S interface
  - Access to General Purpose DMA
- Three I^2C interfaces, SSP, SSP/SPI interfaces
- Four 16C550-type UARTs
  - Includes fractional baud rate generator, auto-baud & hardware flow control

LPC247x Peripherals (continued)

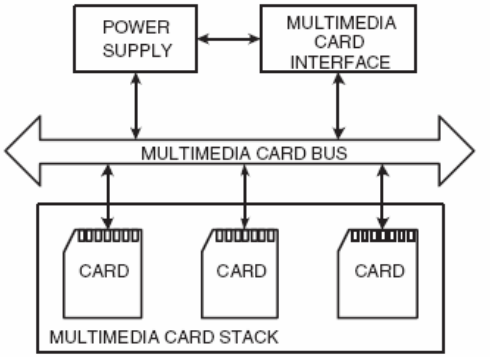
- SD/MMC memory card interface
  - Access to General Purpose DMA
- 8-channel, 10-bit A/D Converter,
- 10-bit D/A Converter
- 4 MHz on-chip RC-oscillator trimmed to 1% accuracy
  - Can be used as Main Clock via PLL
- Four 32-bit general purpose timers
  - Each with 4 Capture, 4 Compare and 4 external outputs
- Watchdog timer from multiple clock source options
- PWM block supporting 3 Phase Motor Control with “dead time” generation
- Low-power Real Time Clock with 2 KB SRAM and battery back-up
- 160 Fast general purpose I/O lines
  - All pins on Port 0 and Port 2 can be used as external interrupts (rising, falling or both)
- Single 3.3V power supply (3.0 to 3.6V)

SD/MMC memory card interface

- Conformance to Multimedia Card Specification v2.11
- Conformance to Secure Digital Memory Card Physical Layer Specification, v0.96
- Use as a multimedia card bus or a secure digital memory card bus host
- It can be connected to several (~4 based on I/O pin loading) multimedia cards, or a single secure digital memory card
- DMA supported through the General Purpose DMA Controller



OR



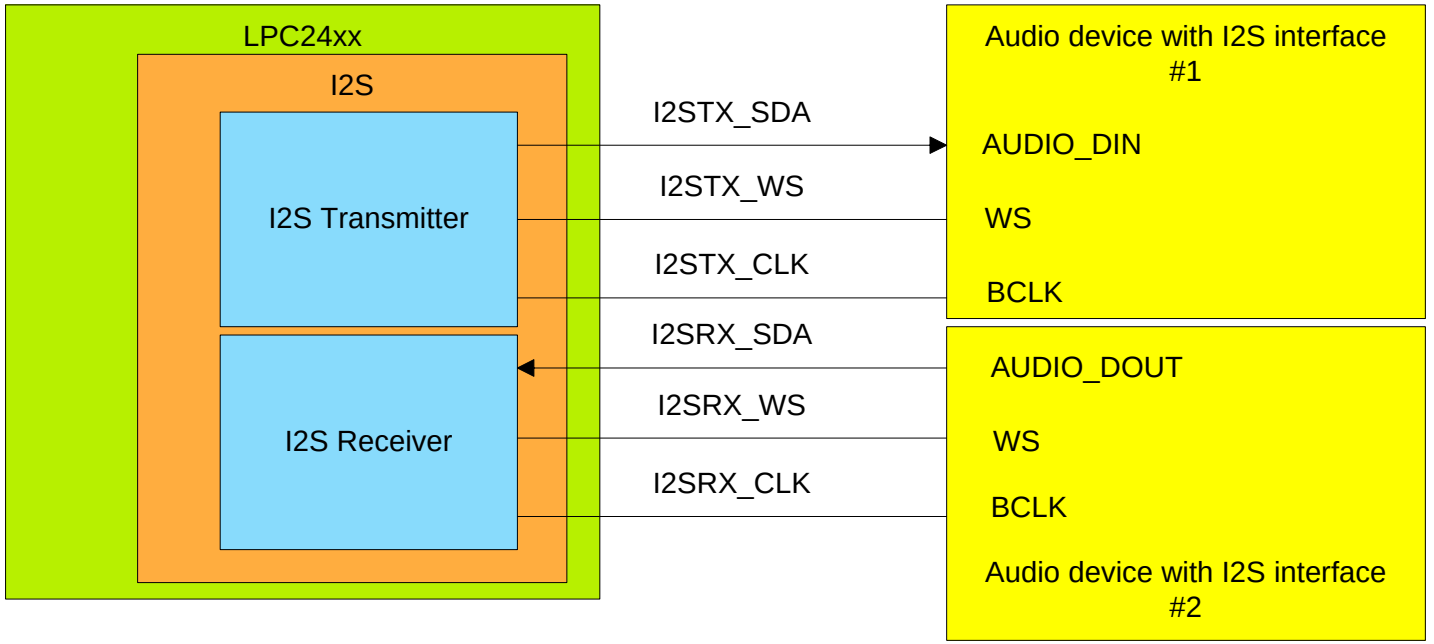
SD/MMC

- SD “Secure Digital” (25Mbit/s)
  - Developed as improvement on MMC
  - Up to 128 Gbyte per card
  - Low speed up to 400Kbit/s
  - High speed up to 100Mbit/s
- MMC “Multi-Media Card” (20Mbit/s)
  - 1, 4, or 8 bits per interface
  - Up to 8Gbyte per card
  - Slightly thinner than SD cards, but pin compatible
- SDIO – small devices that use the SD physical format for other functions beyond storage
  - GPS, WiFi, BlueTooth, Modems, FM Radio, RFID, Barcode, etc., etc.
  - Additional interconnect functionality required
  - May require interrupt line (SD interface does not provide)

I²S Audio Interface

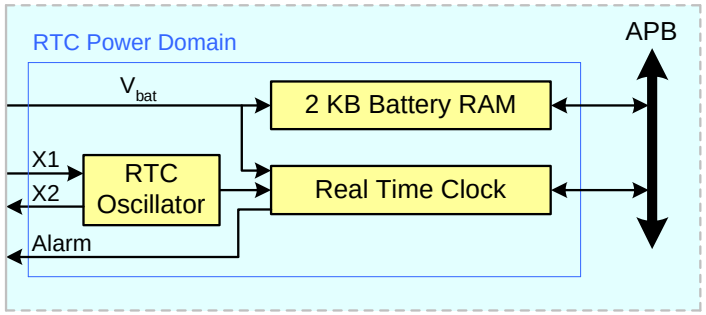
- The I²S bus provides a standard communication interface for digital audio applications
- The I²S bus specification defines a 3-wire serial bus, having 1 data, 1 clock, and one word select signal. The basic I²S connection has one master, which is always the master, and one slave. The I²S interface on the LPC2300/2400 provides a separate transmit and receive channel, each of which can operate as either a master or a slave
- The I²S interface can transmit and receive 8, 16 or 32 bits stereo or mono audio information
- Demo is available for the LPC2300/2400 showing streaming digital Audio concurrent with streaming USB Isochronous data, and Ethernet service of internal web page controlling Dev Board functionality (Keil MCB2370 dev board)

LPC2400 I²S connections



- Four I²S devices: I²S transmitter, I²S receiver, ext. audio device 1 & ext. audio device 2.
- The on-chip I²S transmitter and I²S receiver works independently on each other.
- For each I²S pair: one master and one slave device

Power Modes



- Power options:
  - On-chip DC-DC converter supplies 1.8V power to all internal logic, except in the RTC power domain.
  - 1.8V power can be supplied from off-chip for some pinouts.

- Power reduction modes:
  - Idle mode: CPU stopped; Peripherals running
  - Sleep mode: All clocks & oscillator off. Flash stays powered for fast wake-up
  - Power Down mode: All clocks & oscillator off. RAM state retained between power cycles

LPC2478 液晶控制接口

LPC247x Color LCD Controller

- Based on the ARM PrimeCell® PL111
- Single and dual panel Super Twisted Nematic (STN) monochrome displays with 4 or 8 bit interfaces.
- Single and dual panel STN color displays.
- Thin Film Transistor (TFT) color displays.
- Resolution up to 1024x768
- 15 level grey-scale, 3375 color STN and 32K color TFT display modes.
- 1, 2 or 4 bits-per-pixel (bpp) monochrome palettes for STN displays.
- 1, 2, 4 or 8bpp color palettes for STN and TFT displays.
- 16 bpp direct true-color for STN and TFT displays.
- 24 bpp direct true-color for TFT displays.
- Hardware Cursor support for single panel displays.
- Resistive Touchscreen capability by using internal ADC with port pins or external switches

LCD controller performance

- The LCD controller is connected to the AHB1 bus, so it processes Frame data independently of the Ethernet (AHB2 bus) and Flash (Local bus)
- Example bandwidth calculations
  - For **320 x 240 display**: 76,800 pixels per frame ((x-bits x 76,800)/8 = # bytes/frame)
  - 4-bits per pixel: 38.4 Kbytes per frame
  - 8-bits per pixel: 76.8 Kbytes per frame
  - 12-bits per pixel: 115.2 Kbytes per frame
  - 16-bits per pixel: 153.6 Kbytes per frame
- LCD refresh rate is 70 Hz = 14.3 ms per frame.
- For 16-bits/pixel - 153.6 Kbytes/ 14.28 ms = 10.76 Mbytes/sec
  - An AHB1 transfer requires 2 clocks to transfer 4 bytes (one 32-bit word)
  - For a 60 MHz clock => 120 MBytes per second.
- So 16-bits/pixel requires:
  - 10.76 MBytes/sec divided by 120 MBytes/sec =
  - **ONLY 9% of the AHB1 bandwidth**

Passive LCD Displays

- STN Passive (Super-Twisted Nematic)

  The term "passive" refers to the method by which an individual pixel is controlled. There is no electronic component at the pixel for a passive display. The LCD glass comprised of only row and column conductors. Since STN displays are simpler they are cheaper but optical performance is not as good as active displays.

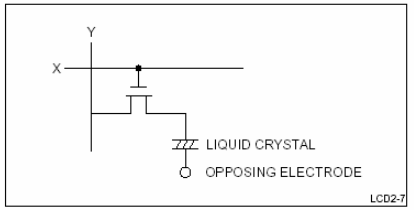
  – Color
    - Size range from 2.4 inches (128X64) to 10.4 inches (640X480)
    - Color depth 2 to 16 bits
    - Connections required (Total of 15 pins)
      5 control signals, 8 data signals, 1 port pin for high voltage control, 1 port pin for backlight on/off or 1 D/A for adjustable backlight

  – Black and white
    - Size range from 2.4 inches (128X64) to 10.4 inches (640X480)
    - Gray scale depth 2-4 bits
    - Connections required (Total of 11 pins)
      5 control signals, 4 data signals, 1 port pin for high voltage control, 1 port pin for backlight on/off or 1 D/A for adjustable backlight

Active LCD Displays

TFT (thin film transistor)

On an active display there is a transistor or diode manufactured into the LCD glass, this provides an "active" element to control the pixel. Active displays have better optical characteristics i.e. Brighter, and better viewing angles. However they consume more power and are more expensive.



- Color
  - Size range from 2.4 inches (128X64) to Big
  - Color depth up to24 bits
  - Connections required (Total of 24 pins for 18 bit, 30 pins for 24 bit)
    5 control signals, 18 data signals for 18 bit, 24 data signals for 24 bit, 1 port pin for backlight on/off or 1 D/A for adjustable backlight.

STN pixel layout

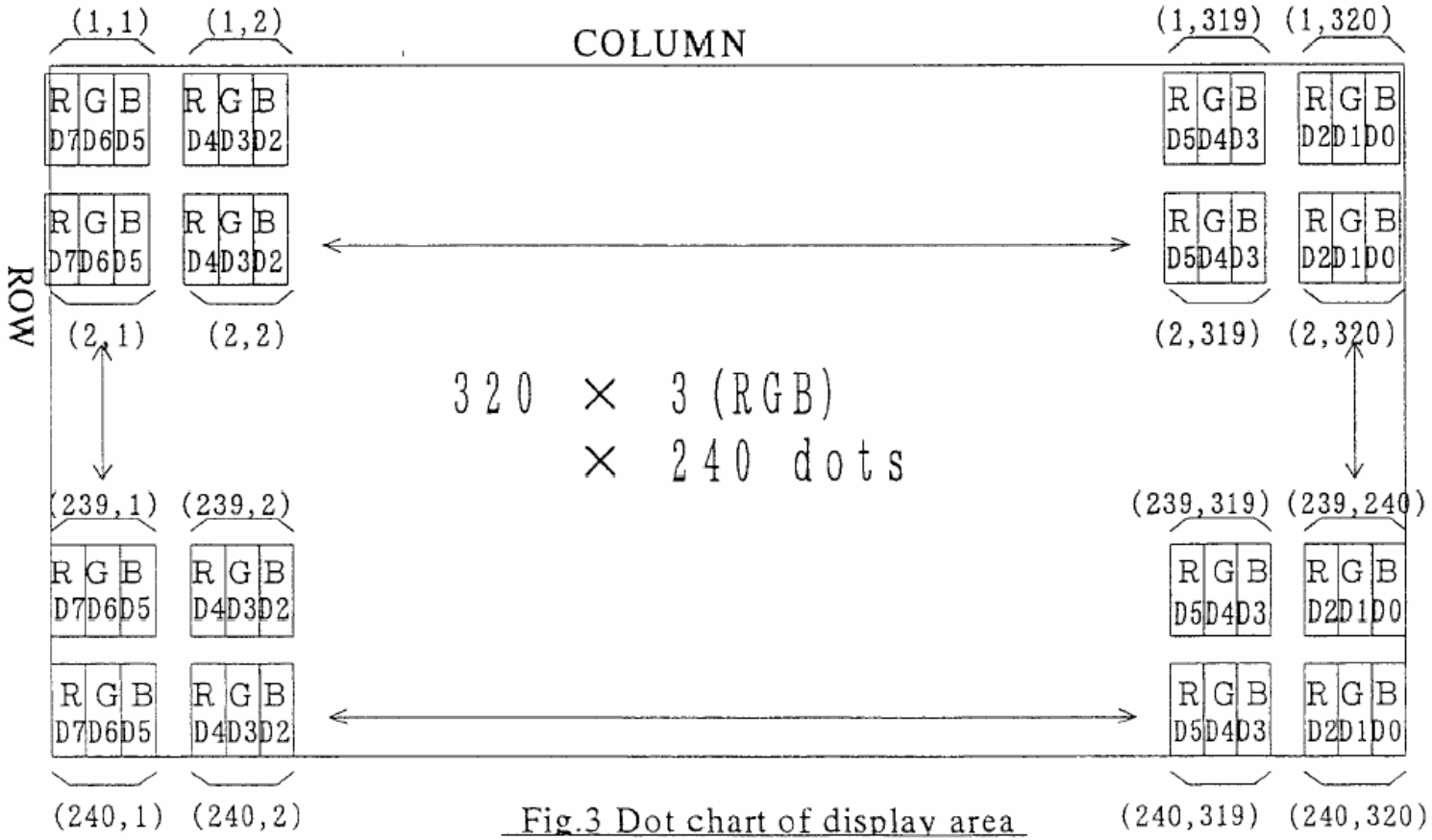


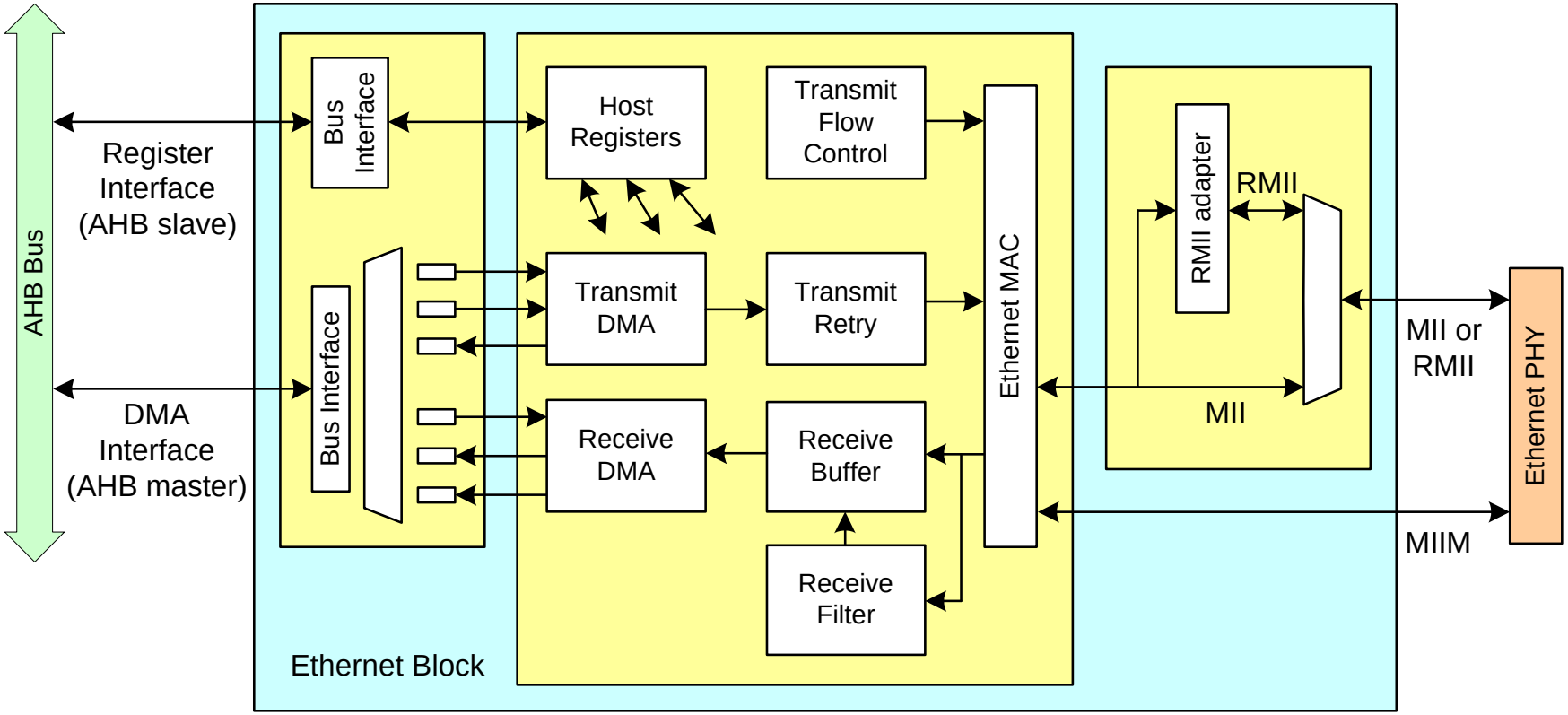
Fig.3 Dot chart of display area

LPC2478以太网接口

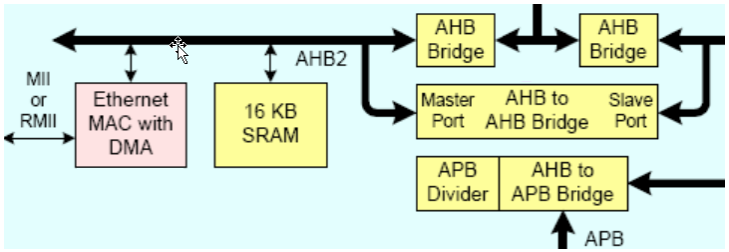
Impact of Ethernet on chip architecture

- Full Duplex point-to-point Ethernet (Link segment or Switched) transfers generates up to 200 Mbits/sec Asynchronous packet traffic
  - 100 Mbits in each direction asynchronous data streams
  - 2 Separate Word transactions every 320 nanoseconds!
  - DMA Channel cannot be allowed to wait for long
  - CPU Bandwidth can be used up very quickly
- The packets need to be streamed into memory:
  - MAC to Receive FIFO via DMA to SRAM to the CPU for processing
  - From the CPU to SRAM to DMA to the Transmit FIFO to MAC
  - Not using DMA makes throughput much worse!
- The following overheads need to be considered:
  - Bus contention between the DMA, CPU, and other Bus masters
  - Bus access and status information overhead and DMA descriptor
  - CPU and DMA memory sharing

Ethernet Block Diagram



Embedded Ethernet



Fast Communications Controller

- Independent, but not isolated second AHB bus
- Supports 10/100 Ethernet PHY devices, including:
  - 10 Base-T
  - 100 Base-TX (Level 5 Unshielded Twisted Pair cable)
  - 100 Base-FX (Fiber Optic cable)
  - 100 Base-T4 (Level 3 UTP cable)
- Reduced Media Independent Interface (RMII) bus (2-bit Data RX/TX paths@50 Mhz): 10 Pins
- Fully Compliant with IEEE 802.3X PAUSE MAC Control protocol
  - Full Duplex Flow Control (prevents the loss of outgoing packets during transmission if the switch is sending packets faster than the attached device can receive and process them by sending pause-control frames when its port buffer becomes full)
  - Half Duplex Back Pressure (ensures retransmission of incoming packets if unable to receive incoming packets)

Enhanced Ethernet Features

- Receive Filtering
- Multicast and broadcast frame support for both transmit and receive and promiscuous receive mode
- Selectable automatic transmit frame padding and reception with Scatter-Gather DMA off-loads many operations from the CPU
- Over-length frame support for both transmit and receive allows any length frames
- Optional automatic Frame Check Sequence insertion (4-byte CRC) for transmit error correction
- Automatic collision backoff and frame retransmission
- Includes power management by clock switching
- Wake-on-LAN power management support allows system wake-up using the receive filters or a magic packet detection filter

External Ethernet PHY

- National Semiconductor's DP838481 PHYTER Family
  - Selectable MII and RMII for design flexibility
  - Full support of JTAG (IEEE 1149.1) for simplified manufacturing
  - Low external component count for easy interface with twisted-pair media
  - Other features include Auto-MDIX, 25 MHZ clock output and low power
  - 48 pin LQFP package
  - http://www.ethernet.national.com
- Other Ethernet PHY
  - Micrel KS8721
  - SMSC LAN83C185
  - TDK 78Q2133
  - Broadcom BCM5220
  - Davicom DM9101

NicheLite for LPC by Interniche

- NicheLite for LPC is a fully featured TCP/IP stack
  - Requires as little as 12 KB of code.
- Includes NicheTask ™ a cooperative multi-tasking scheduler.
- Supports InterNiche's Light Weight API and a Zero-Copy option.
- Single Ethernet interface with device drivers optimized for the LPC2300 and LPC2400
- Example applications (TFTP Client, TFTP Server, HTTP Listener)
- Support from Interniche at sales@interniche.com
- License - Unlimited use of source code with NXP LPC2000 and LPC3000 microcontrollers only

LPC2478 USB接口

LPC247x has Fully-Compliant USB2.0

		USB 2.0 Standard	NXP LPC2000	STR7X	ML671xx	SAM7S
Bidirectional Endpoints supported:		16	16	8	3	2
Modes:	Control	Y	Y	Y	Y	Y
	Interrupt	Y	Y	Y	Y	Y
	Bulk	Y	Y	Y	Y	Y
	Isochronous	Y	Y	Y	Y	-
Maximum:	Control Buffer Size	64	64	64	64	64
	Interrupt Buffer Size	64	64	64	64	64
	Bulk Buffer Size	64	64	64	64	64
	Isoch. Buffer Size	1023X2	1023X2	256X2	256X2	None
Frame BW per Transfer		69%	69%	9%	9%	N/A
AHB Bus Access			Yes(DMA)	No (APB)	APB w DMA	No (APB)

LPC2000 USB enables 8.3 Mb/s data throughput

Others can only achieve ~ 1Mb/s

USB Host/ On-The Go

- USB Host
  - Enables full- and low-speed data exchange with USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller
  - OHCI compliant
  - Two downstream ports
  - Supports per-port power switching
- USB OTG
  - Integrates the host controller, device controller, and a master-only I2C interface to implement OTG dual-role device functionality. The dedicated I2C interface controls an external OTG transceiver
  - Fully compliant with On-The-Go supplement to the USB 2.0 Specification
  - Hardware support for Host Negotiation Protocol (HNP).
  - Includes programmable timer for HNP and Session Request Protocol (SRP)
  - Supports any OTG transceiver compliant with the OTG Transceiver Specification

Flexible Clocking Scheme

- Two separate PLL's provide lot of flexibility to the user to run the core and the USB independently at different speeds
- Considering the three possible option
  - Crystal Frequency –12MHz
    - Core Freq= 12,24,36,48,60MHz
    - USB Freq =48MHz
  - Crystal Frequency –16MHz
    - Core Freq= 16,32,48MHz
    - USB Freq =48MHz
  - Crystal Frequency –24MHz
    - Core Freq= 24,48MHz
    - USB Freq =48MHz

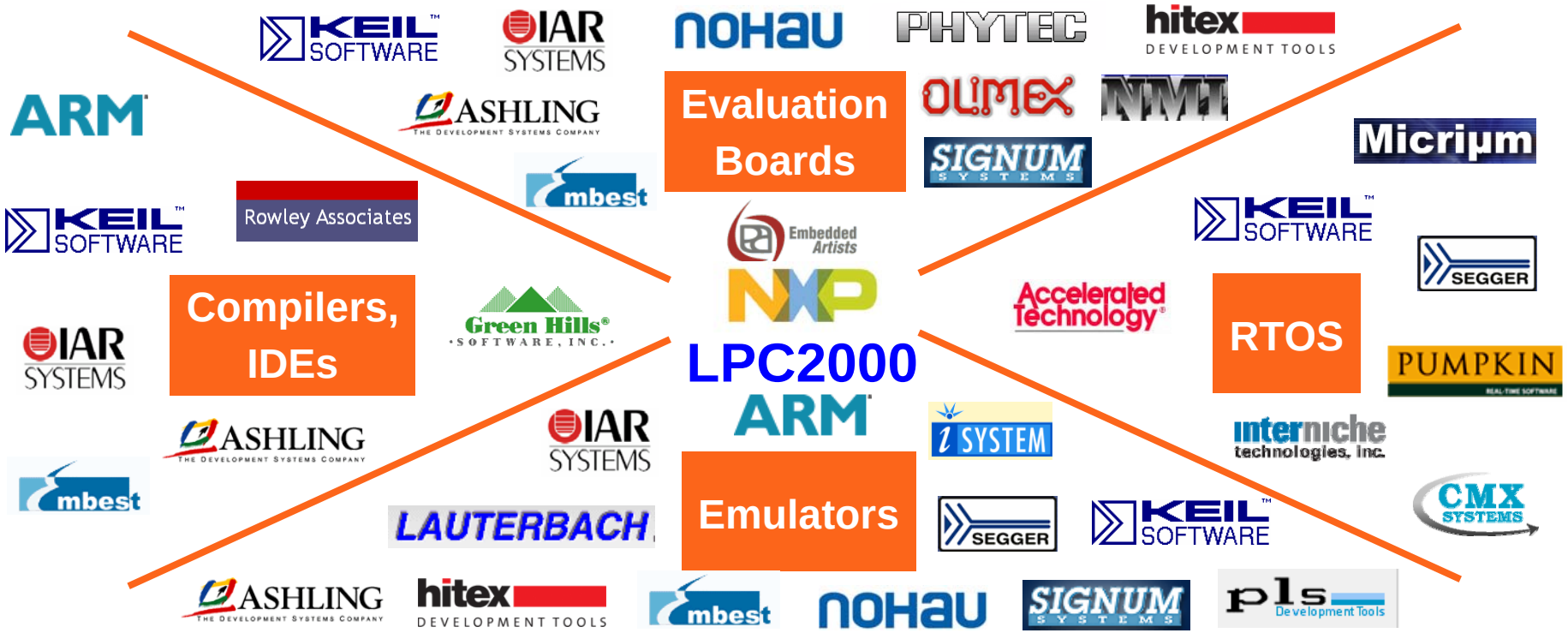
Fastest USB operation available at any CPU frequency

LPC2478开发工具

LPC2000 Development Tools

Available from traditional 8-bit tool providers as well as established 32-bit providers

- Low cost evaluation kits – Starting at $99!
  - IAR Kickstart kits with free 32K compiler
  - Keil evaluation kits with free 16K compiler

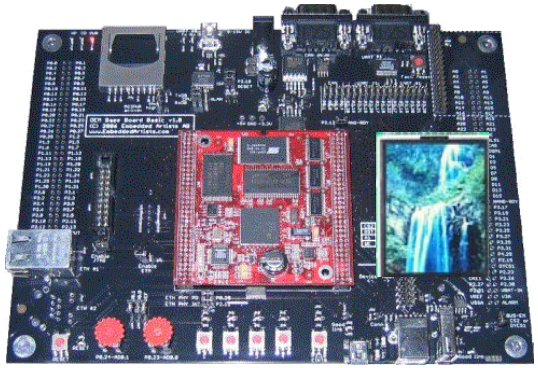


Development Tools

- Standard ARM JTAG interface compatible with all major ARM tool chains
- Real-Time Emulation Trace Interface
- Real Monitor On-chip Background Debugger for non-invasive Debug (CPU not forced to stop for Debug)
- Development Boards available from Keil (ARM)
- Free FlashMagic Flash download program supports LPC247x
  - http://www.esacademy.com/software/flashmagic

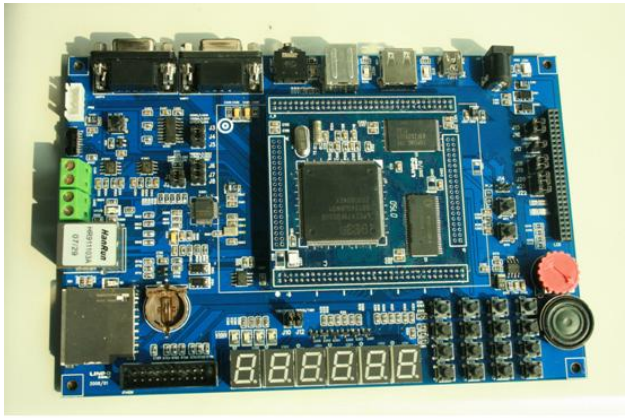
Embedded Artists LPC2478 OEM Board

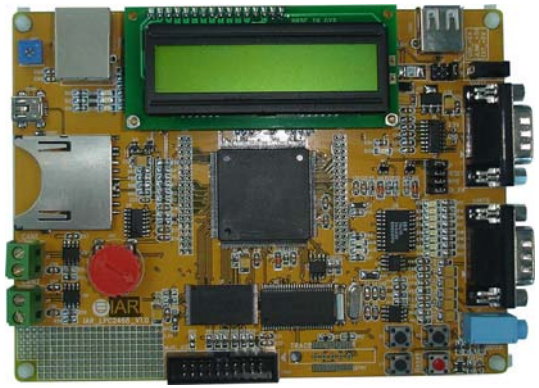
- LPC2478 in BGA, Small form factor board (70 x 66 mm)
- 100/10Mbps Ethernet PHY
- 256 Mbit SDRAM, 1 Gbit NAND FLASH, 32 Mbit NOR FLASH, 256 Kbit EEPROM
- Ethernet connector, USB OTG/Host/Device connectors, MMC/SD connector, CAN interface and connector, JTAG and ETM connectors
- USB-to-serial bridge (UART #0), Full modem RS232 on UART #1
- Keys/LEDs via I2C
- Power supply
- 192 pin expansion connector (2 mm pitch)
  - QVGA expansion
  - WLAN expansion

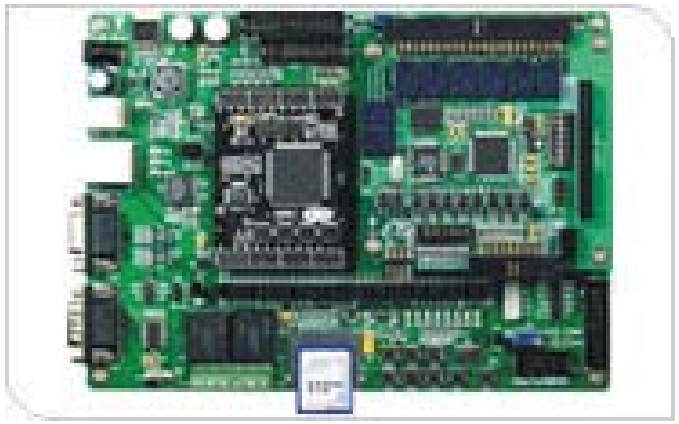


Local Supplier for LPC2478 demo board

- Zhiyuan
- Linpo
- Polar
- uCDragon







LPC2478 技术支持

Reminder: FlashMagic now supports LPC2000

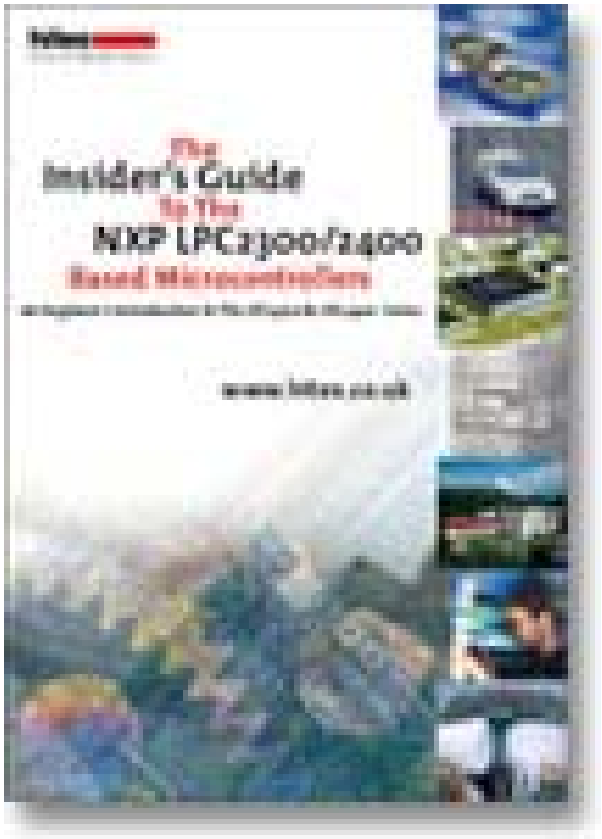
- During 2006, we worked with Embedded Systems Academy to integrate our ARM7 LPC2000 family into their **FlashMagic** ISP tool which is already the ISP tool of choice for our LPC900 and our flash-based 8051 products. FlashMagic can be downloaded for free here:
- http://www.flashmagictool.com/
- FlashMagic supports all LPC2000 devices with on-chip flash, including the LPC2300 devices and the LPC2468.
- All future LPC2000 devices will be supported by FlashMagic only. The Philips LPC2000 Flash ISP Utility was an in-house solution and will **no longer** be maintained.

Filterable Product Selector Guide
- for all Multimarket Semiconductors

http://www.standardics.nxp.com/support/software/selector/

Insider's Guide to LPC2000

- 200 page guide to LPC2000 featuring chapters on:
  - ARM7 Core
  - Software Development
  - System Peripherals
  - User Peripherals
  - Keil Tutorial
  - GNU Tutorial
- Perfect for engineers without ARM experience
- Updated for LPC2300/2400



http://www.hitex.co.uk/download/docs/lpc2300/con-reg-download-lpc2300-book.html
http://www.hitex.co.uk/arm/lpc2000book/book_downloadform.html

Important Links

- Yahoo User Group on LPC2000
  - http://groups.yahoo.com/group/lpc2000/
- LPC2000 Tips
  - http://www.open-research.org.uk/ARMuC/index.cgi?LPC2100Tips
- Another LPC2000 Forum
  - http://www.sparkfun.com/cgi-bin/phpbb/viewforum.php?f=11
- Errata
  - http://www.standardics.nxp.com/support/documents/microcontrollers/?type=errata
- LPC Tools – Order select tools and more…
  - http://www.lpctools.com/
- Embedded Systems Academy – training courses and sample code
  - http://www.esacademy.com/

LPC2000 User's Group
Over 5800 members worldwide!

Activity within 7 days: 53 New Members - 1 New Link - 203 New Messages - 7 New Files

Description

The NXP (formerly Philips) LPC2000 family of ARM MCUs is sufficiently different from other ARM variants that I decided that a forum dedicated to it would be useful.

Info | Settings

Group Information

Members: 5847

Category: Microcontrollers

Founded: Nov 17, 2003

Language: English

Message History

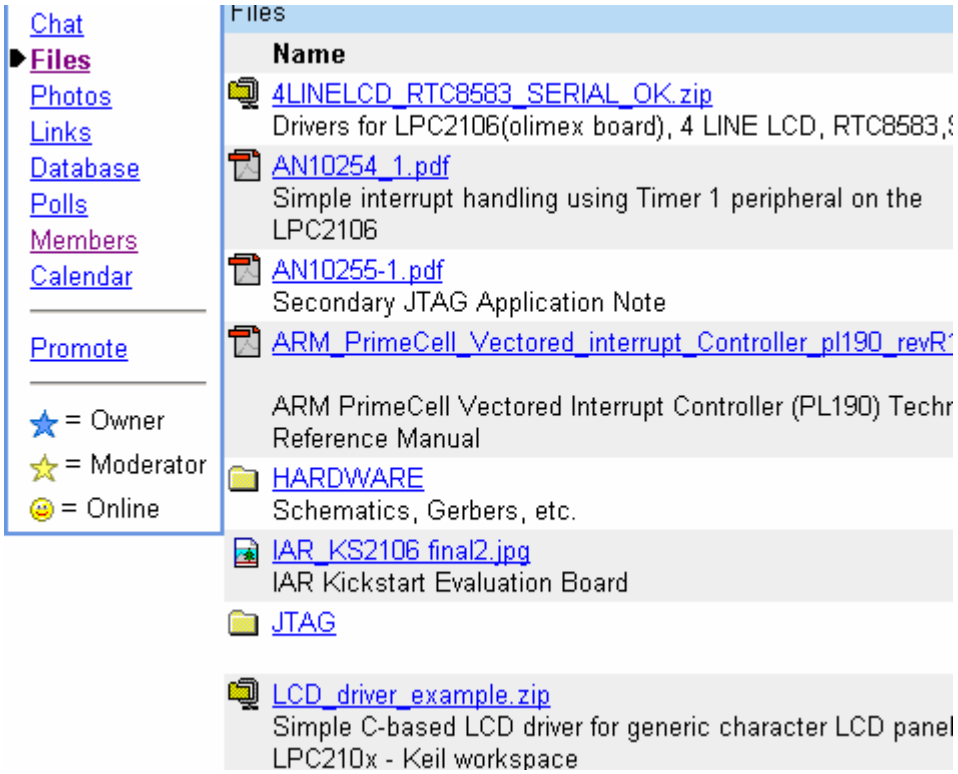
	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
2008	631	538										
2007	776	631	807	733	578	551	613	719	850	1083	740	592
2006	1039	930	1041	903	730	701	911	814	702	640	764	575
2005	592	577	551	550	385	436	418	377	471	754	1072	896
2004	328	545	344	286	364	335	322	178	299	427	393	571
2003											113	308

http://groups.yahoo.com/group/lpc2000/

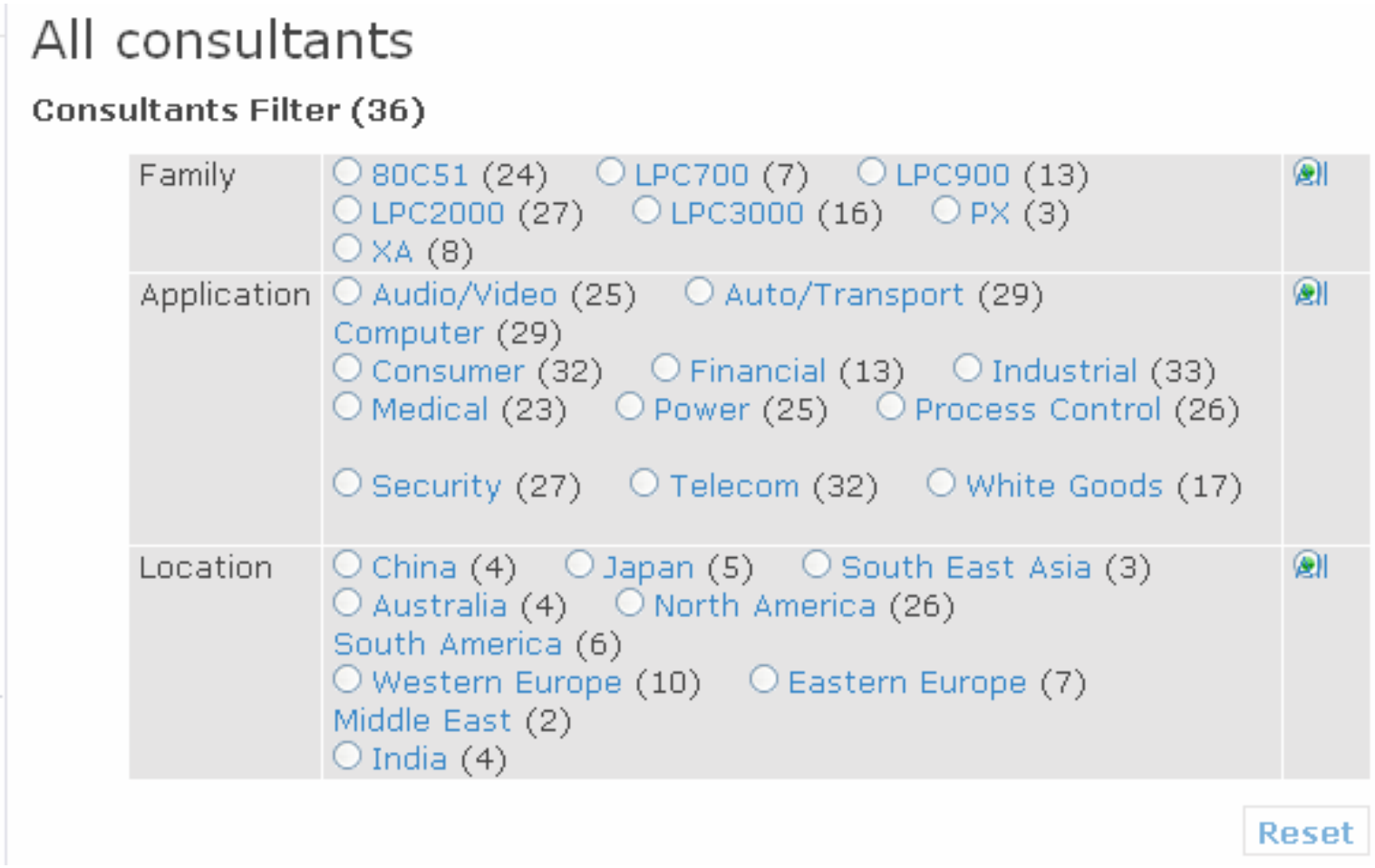
LPC2000 forum- Files

YAHOO! Groups

- Various drivers
- Software Examples
- LPC based Application notes
- VB applications
- Board Schematics

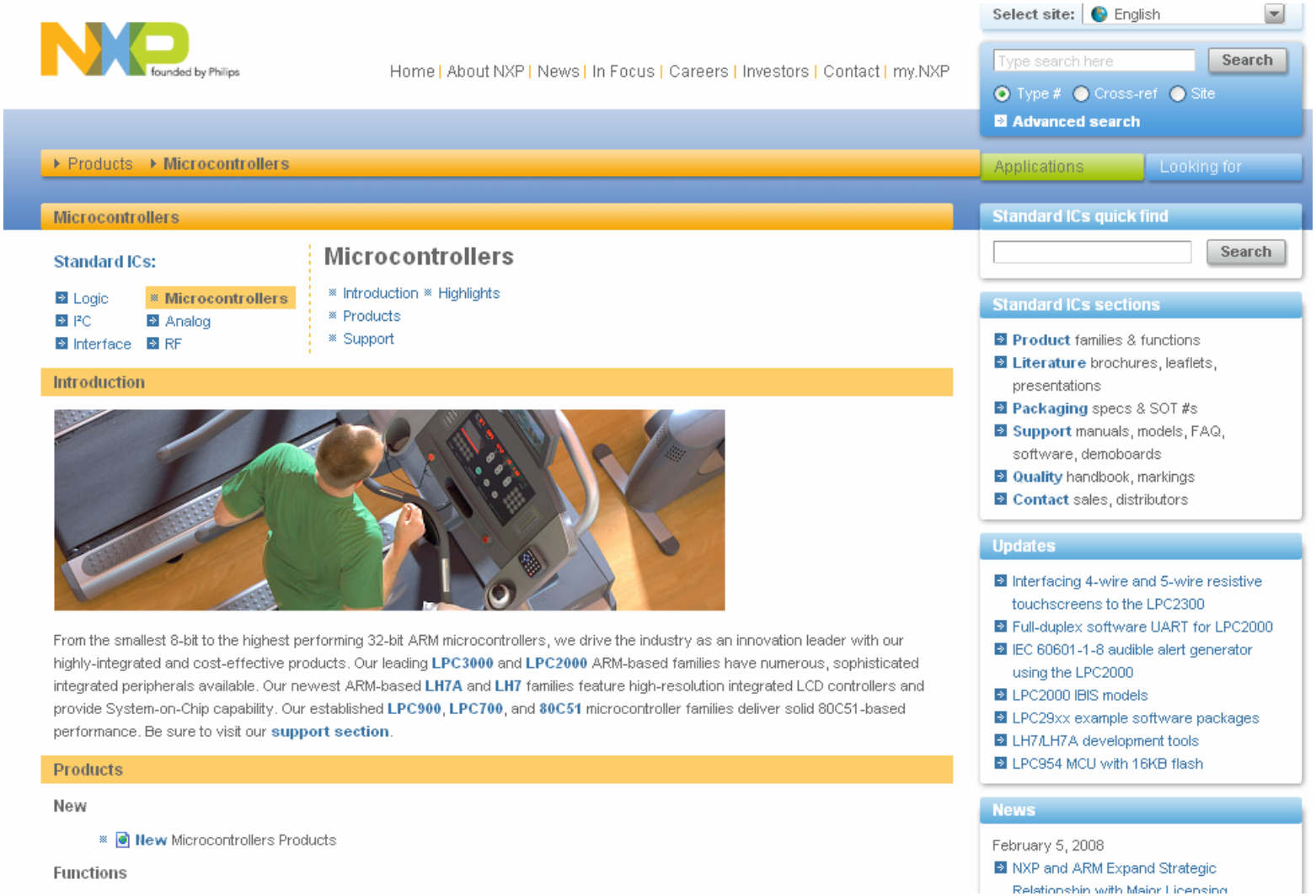


MCU Consultants Site



http://www.StandardICs.NXP.com/support/consultants/microcontrollers/

http://www.nxp.com/microcontrollers



Thanks!